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Apparatus for Loose Register Encoding Within a Pipelined Processor" filed contemporaneously herewith and incorporated by reference in its entirety herein, may be used in conjunction with the jump delay slot invention described herein.--

IN THE CLAIMS

Please cancel Claims 6-13, 21-22, and 24 without prejudice, and amend Claims 1, 14, 17, 20, and 23 as follows:

B5 Sub D1

1. A method of controlling the execution of instructions within a pipelined processor, comprising:

providing an instruction set comprising a plurality of instruction words, each of said instruction words comprising a plurality of data bits, at least one of said words comprising a jump instruction having at least one user-configurable mode associated therewith;

assigning one of a plurality of values to at least one of said data bits of said at least one jump instruction; and

controlling the execution of at least one subsequent instruction within said pipeline based on said one assigned value of said at least one data bit when said at least one jump instruction is decoded.

B6 Sub D2

14. A digital processor comprising:

a processor core having a multistage instruction pipeline, said core being adapted to decode and execute an instruction set comprising a plurality of instruction words;

a data interface between said processor core and an information storage device; and

an instruction set comprising a plurality of instruction words, at least one of said instruction words being a user-configurable jump instruction containing data defining a plurality of jump delay slot modes, said plurality of modes controlling the execution of instructions within said instruction pipeline of said processor core in response to said at least one jump instruction word within said instruction set.

B7 Sub 01

17. A digital processor having at least one pipeline and an associated data storage device, wherein the execution of instructions within said at least one pipeline is controlled by the method comprising:

storing an instruction set within said data storage device, said instruction set comprising a plurality of instruction words, each of said instruction words comprising a plurality of data bits, at least one of said instruction words comprising a user-configurable branch instruction directing branching to a first address within said data storage device;

assigning one of a plurality of values to [at least one] each of said data bits of said at least one branch instruction;

decoding said at least one branch instruction including said one [value] values;

determining whether to execute an instruction within said pipeline in a stage preceding that of said at least one branch instruction based at least in part on said one [value] values; and

branching to said first address based on said at least one branching instruction.

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20. A method of controlling [the branching within the] program operation of a multi-stage pipelined digital processor, comprising:

storing an instruction set within said data storage device, said instruction set comprising a plurality of instruction words, each of said instruction words comprising a plurality of data bits, at least one of said instruction words comprising a branch instruction directing branching to a first address within said data storage device based on a first parameter;

defining a plurality of jump delay slot modes comprising;

(i) executing a subsequent instruction under all circumstances;

(ii) executing a subsequent instruction only if jumping occurs;

(iii) stalling the pipeline for one cycle if jumping occurs; and

(iv) stalling the pipeline for two or more cycles if jumping occurs;

assigning at least one of said plurality of jump modes to at least [one] two of said data bits of said at least one branch instruction;

decoding said at least one branch instruction including said at least [one] two data bits; and

[determining whether to branch to said first address based on said at least one data bit and said first parameter] controlling said pipeline based at least in part on said at least two data bits and said first parameter.

23. A digital processor comprising:

processing means having a multistage data pipeline, said processing means being adapted to decode and execute an instruction set comprising a plurality of instruction words;

means for storing data;

data interface means for transferring data between said processing means and said means for storing data; and

an instruction set comprising a plurality of instruction words, at least one of said instruction words being a user-configurable jump instruction containing data defining a plurality of jump control means, said plurality of jump control means controlling the execution of instructions within said data pipeline of said processing means in response to said at least one jump instruction word within said instruction set.

Please add new Claims 33-43 as follows:

33. A method of controlling the execution of instructions within a user-configured pipelined processor, comprising:

providing an instruction set comprising a plurality of instruction words, each of said instruction words comprising a plurality of data bits, at least one of said words comprising a branch instruction having at least one user-configurable mode and a plurality of other modes adapted for controlling the execution of at least one subsequent instruction;

assigning one of a plurality of values to at least one of said data bits of said at least one branch instruction; and

controlling the execution of at least one subsequent instruction within said pipeline based on said one assigned value of said at least one data bit when said at least one branch instruction is decoded.

34. A method of controlling the execution of instructions within a pipelined processor, comprising:

providing an instruction set comprising a plurality of instruction words, each of said instruction words comprising a plurality of data bits, at least one of said words comprising a jump instruction;

assigning one of a plurality of values to first and second of said data bits of said at least one jump instruction, said first and second bits adapted to define four discrete jump modes; and

controlling the execution of at least one subsequent instruction within said pipeline based on said assigned values of said first and second data bits when said at least one jump instruction is decoded.

35. A method of controlling the execution of instructions within a pipelined processor, comprising:

providing an instruction set comprising a plurality of instruction words, each of said instruction words comprising a plurality of data bits, at least one of said words comprising a jump instruction;

assigning one of a plurality of values to first and second of said data bits of said at least one jump instruction, said first and second bits adapted to define four discrete jump modes, said four discrete jump modes including one user-defined jump mode; and

controlling the execution of at least one subsequent instruction within said pipeline based on said assigned values of said first and second data bits when said at least one jump instruction is decoded.

36. A digital processor having at least one pipeline and an associated data storage device containing at least a portion of an instruction set comprising a plurality of instruction words, each of said instruction words comprising a plurality of data bits, at least one of said words comprising a jump instruction, wherein the execution of instructions within said at least one pipeline is controlled by (i) the assignment of one of a plurality of values to first and second of said data bits of said at least one jump instruction, said first and second bits adapted to define four discrete jump modes; and (ii) the execution of at least one subsequent instruction within

said pipeline based on said assigned values of said first and second data bits, when said at least one jump instruction is decoded.

37. An extensible pipelined digital processor having an instruction set comprising a plurality of basecase instructions and at least one extension instruction, at least one of said basecase and extension instructions comprising a branch instruction having at least one user-configurable mode and a plurality of other modes controlling the execution of at least one instruction in a delay slot following said branch instruction within said pipeline.

38. An extensible pipelined digital processor having an instruction set comprising a plurality of basecase instructions and at least one extension instruction, at least one of said basecase and extension instructions comprising a branch instruction including two data bits defining four discrete modes controlling the execution of at least one instruction in a delay slot following said branch instruction within said pipeline.

39. An extensible pipelined digital processor having an instruction set, said processor comprising:

a basecase processor core configuration including a base instruction set; and

at least one user-configured extension instruction within said instruction set, said at least one extension instruction comprising a branch instruction having at least one user-defined mode and a plurality of other modes controlling the execution of at least one instruction in a delay slot following said branch instruction within said pipeline.

40. An extensible pipelined digital processor having basecase and extension instruction sets, at least one instruction within said basecase set comprising a branch instruction having at least four discrete modes for controlling the execution of at least one instruction in a delay slot following said branch instruction within said pipeline, said processor comprising:

a basecase processor core configuration including said base instruction set; and

at least one user-customized extension instruction within said instruction set.

41. A digital processor having at least one pipeline and an associated data storage device containing at least a portion of an instruction set comprising a plurality of instruction words, each of said instruction words comprising a plurality of data bits, at least one of said words comprising a branch instruction, wherein the execution of instructions within said at least